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Reissue of U.S. Patent 6,324,639

AMENDMENT TO THE CLAIMS

34-39. (Canceled)

40. (Three times amended) A processor comprising:

an execution unit capable of executing up to N number of instructions having a variable bit length in parallel, N being an integer which is at least two, wherein the maximum bit length of an instruction that is executed in parallel is M bits, M being an integer;

an instruction supplying/issuing unit which fetches an instruction sequence in a unit of a first bit length of code and outputs the instruction sequence in a unit of a second bit length of code;

a decoding unit which decodes the instruction sequence in a unit of a variable bit length of code which is at least a part of the second bit length of code outputted by the instruction supplying/issuing unit, and outputting a decoding result to the execution unit; and

an instruction bus formed between the instruction supplying/issuing unit and the decoding unit, wherein the total bit width of the instruction bus is shorter than $M * N$ bits,

wherein the decoding unit is capable of decoding a plurality of instructions executed in parallel.

41. (New) The processor of claim 40,

wherein the instruction sequence is converted by a certain instruction conversion apparatus.

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42. (New) The processor of claim 41,
wherein the instruction sequence is written in a high-level language before being
converted by the instruction conversion apparatus.
43. (New) The processor of claim 40,
wherein the first bit length is shorter than the second bit length.
44. (New) The processor of claim 40,
wherein at least a part of the instructions have a special bit which instructs the target
processor to execute a plurality of instructions in parallel.
45. (New) The processor of claim 40,
wherein the decoding unit comprises:
an instruction issuing control unit which identifies instruction boundaries executed in
parallel.
46. (New) The processor of claim 40,
wherein instruction supplying/issuing unit comprising:
a fetch unit for successively fetching the instruction sequence; and
a plurality of instruction buffers for temporally storing instructions.

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47. (Currently amended) A processor comprising:

an instruction fetching unit that fetches instructions, each instruction having a variable bit length, wherein the maximum bit length of an instruction that is executed in parallel is M bits, M being an integer;

a decoding unit that decodes a plurality of instructions executed in parallel;

an execution unit capable of executing up to N number of decoded instructions from the decoding unit in parallel, N being an integer which is at least two; and

an instruction bus formed between the instruction supplying/issuing unit and the decoding unit, wherein the total bit width of the instruction bus is shorter than $M * N$ bits,

wherein the total bit length of the decoded instructions that are executed in parallel is variable which is not related to the bit length of the fetched instructions.

48. (New) The processor of claim 47,

wherein the instruction sequence is converted by a certain instruction conversion apparatus.

49. (New) The processor of claim 48,

wherein the instruction sequence is written in a high-level language before being converted by the instruction conversion apparatus.

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50. (New) The processor of claim 47,
wherein the instruction fetching unit fetches an instruction sequence in a unit of a first bit
length of code and outputs the instruction sequence in a unit of a second bit length of code, the
first bit length being shorter than the second bit length.

51. (New) The processor of claim 47,
wherein at least a part of the instructions have a special bit which instructs the target
processor to execute a plurality of instruction in parallel.

52. (New) The processor of claim 47,
wherein the decoding unit comprises:
an instruction issuing control unit which identifies instruction boundaries executed in
parallel.

53. (New) The processor of claim 47, further comprising:
a plurality of operation execution units capable of executing a plurality of instructions in
parallel in accordance with a decoding result of the decoding unit.

54. (New) The processor of claim 47,
wherein instruction fetching unit comprising:
a fetch unit for successively fetching the instruction sequence; and
a plurality of instruction buffers for temporally storing instructions.